LISTING OF THE CLAIMS

1. (original) A method for fabricating a semiconductor substrate comprising:

defining a sequential and repetitive thermal oxidation and partial stripping method for forming upon a semiconductor substrate a plurality of gate dielectric layers having a maximum numbered plurality of differing thicknesses formed employing a corresponding maximum numbered plurality of thermal oxidation process steps;

sequentially and repetitively thermally oxidizing and partially stripping the semiconductor substrate to form thereupon the plurality of gate dielectric layers having less than the maximum numbered plurality of differing thicknesses formed employing less than the corresponding maximum numbered plurality of thermal oxidation process steps; and

supplementally thermally annealing the semiconductor substrate to compensate for forming thereupon the plurality of gate dielectric layers having less than the corresponding maximum numbered plurality of differing thicknesses formed employing less than the corresponding maximum numbered plurality of thermal oxidation process steps.

2. (original) The method of claim 1 wherein the maximum numbered plurality is at least three.

3. (original) The method of claim 1 wherein the maximum numbered plurality is greater than three.

4. (original) The method of claim 1 wherein the plurality of differing thicknesses encompass a range including a low thickness of from about 10 to about 40 angstroms and a high thickness of from about 50 to about 200 angstroms.

5. (original) The method of claim 1 wherein the supplemental thermal annealing is undertaken prior to forming the plurality of gate dielectric layers upon the semiconductor substrate.

6. (original) The method of claim 1 wherein the supplemental thermal annealing is undertaken interposed between forming the plurality of gate dielectric layers upon the semiconductor substrate.

7. (original) The method of claim 1 wherein the supplemental thermal annealing is undertaken subsequent to forming the plurality of gate dielectric layers upon the semiconductor substrate.

8. (original) A method for fabricating a semiconductor substrate comprising:

defining a sequential and repetitive thermal oxidation and partial stripping method for forming upon a semiconductor substrate a plurality of gate dielectric layers having three differing thicknesses formed employing three thermal oxidation process steps;

sequentially and repetitively thermally oxidizing and partially stripping the semiconductor substrate to form thereupon the plurality of gate dielectric layers having less than the three differing thicknesses formed employing less than the three thermal oxidation process steps; and

supplementally thermally annealing the semiconductor substrate to compensate for forming thereupon the plurality of gate dielectric layers having the less than three differing thicknesses formed employing the less than three thermal oxidation process steps.

9. (original) The method of claim 8 wherein the plurality of differing thicknesses encompass a range including a low thickness of from about 10 to about 40 angstroms and a high thickness of from about 50 to about 200 angstroms.

10. (original) The method of claim 8 wherein the supplemental thermal annealing is undertaken prior to forming the plurality of gate dielectric layers upon the semiconductor substrate.

11. (original) The method of claim 8 wherein the supplemental thermal annealing is undertaken interposed between forming the plurality of gate dielectric layers upon the semiconductor substrate.

12. (original) The method of claim 8 wherein the supplemental thermal annealing is undertaken subsequent to forming the plurality of gate dielectric layers upon the semiconductor substrate.

13. (previously added) A method for fabricating a semiconductor substrate comprising:

defining a sequential and repetitive thermal oxidation and partial stripping method for forming upon a semiconductor substrate a plurality of gate dielectric layers having a maximum numbered plurality of differing thicknesses formed employing a corresponding maximum numbered plurality of thermal oxidation process steps;

sequentially and repetitively thermally oxidizing and partially stripping the semiconductor substrate to form thereupon the plurality of gate dielectric layers having less than the maximum numbered plurality of differing thicknesses formed employing less than the corresponding maximum numbered plurality of thermal oxidation process steps; and

supplementally thermally annealing the semiconductor substrate without forming a gate dielectric layer thereupon to compensate for forming thereupon the plurality of gate dielectric layers having less than the corresponding maximum numbered plurality of differing thicknesses formed employing less than the corresponding maximum numbered plurality of thermal oxidation process steps.

14. (previously added) The method of claim 1 wherein the maximum numbered plurality is at least three.

5. (original) The method of claim 1 wherein the supplemental thermal annealing is undertaken prior to forming the plurality of gate dielectric layers upon the semiconductor substrate.

6. (original) The method of claim 1 wherein the supplemental thermal annealing is undertaken interposed between forming the plurality of gate dielectric layers upon the semiconductor substrate.

7. (original) The method of claim 1 wherein the supplemental thermal annealing is undertaken subsequent to forming the plurality of gate dielectric layers upon the semiconductor substrate.

8. (original) A method for fabricating a semiconductor substrate comprising:

defining a sequential and repetitive thermal oxidation and partial stripping method for forming upon a semiconductor substrate a plurality of gate dielectric layers having three differing thicknesses formed employing three thermal oxidation process steps;

sequentially and repetitively thermally oxidizing and partially stripping the semiconductor substrate to form thereupon the plurality of gate dielectric layers having less than the three differing thicknesses formed employing less than the three thermal oxidation process steps; and

supplementally thermally annealing the semiconductor substrate to compensate for forming thereupon the plurality of gate dielectric layers having the less than three differing thicknesses formed employing the less than three thermal oxidation process steps.

9. (original) The method of claim 8 wherein the plurality of differing thicknesses encompass a range including a low thickness of from about 10 to about 40 angstroms and a high thickness of from about 50 to about 200 angstroms.

10. (original) The method of claim 8 wherein the supplemental thermal annealing is undertaken prior to forming the plurality of gate dielectric layers upon the semiconductor substrate.

11. (original) The method of claim 8 wherein the supplemental thermal annealing is undertaken interposed between forming the plurality of gate dielectric layers upon the semiconductor substrate.

12. (original) The method of claim 8 wherein the supplemental thermal annealing is undertaken subsequent to forming the plurality of gate dielectric layers upon the semiconductor substrate.

13. (previously added) A method for fabricating a semiconductor substrate comprising:

defining a sequential and repetitive thermal oxidation and partial stripping method for forming upon a semiconductor substrate a plurality of gate dielectric layers having a maximum numbered plurality of differing thicknesses formed employing a corresponding maximum numbered plurality of thermal oxidation process steps;

sequentially and repetitively thermally oxidizing and partially stripping the semiconductor substrate to form thereupon the plurality of gate dielectric layers having less than the maximum numbered plurality of differing thicknesses formed employing less than the corresponding maximum numbered plurality of thermal oxidation process steps; and

supplementally thermally annealing the semiconductor substrate without forming a gate dielectric layer thereupon to compensate for forming thereupon the plurality of gate dielectric layers having less than the corresponding maximum numbered plurality of differing thicknesses formed employing less than the corresponding maximum numbered plurality of thermal oxidation process steps.

14. (previously added) The method of claim 1 wherein the maximum numbered plurality is at least three.

15. (previously added) The method of claim 1 wherein the maximum numbered plurality is greater than three.

16. (previously added) The method of claim 1 wherein the plurality of differing thicknesses encompass a range including a low thickness of from about 10 to about 40 angstroms and a high thickness of from about 50 to about 200 angstroms.

17. (previously added) The method of claim 1 wherein the supplemental thermal annealing is undertaken prior to forming the plurality of gate dielectric layers upon the semiconductor substrate.

18. (previously added) The method of claim 1 wherein the supplemental thermal annealing is undertaken interposed between forming the plurality of gate dielectric layers upon the semiconductor substrate.

19. (previously added) The method of claim 1 wherein the supplemental thermal annealing is undertaken subsequent to forming the plurality of gate dielectric layers upon the semiconductor substrate.